Birla Institute of Technology & Science, Pilani
Hyderabad Campus

CALL FOR JUNIOR RESEARCH FELLOW FOR AN INDUSTRY FUNDED PROJECT

Date: 12th July, 2022

Applications are invited from suitable candidates for two **Junior Research Fellow (JRF)** positions to work on an Industry (Ceremorphic, Inc) sponsored project under the supervision of **Dr. Parikshit Sahatiya (PI)**, Assistant Professor, **Prof. Surya Shankar Dan (Co-PI)**, Associate Professor, **Dr. Subhradeep Pal (Co-PI)**, Assistant Professor, Department of Electrical and Electronics Engineering (EEE), BITS Pilani, Hyderabad campus. Both the candidates are expected to work in a broad multidisciplinary environment involving fabrication, characterization, ~~and~~ developing data driven models using machine learning (ML), to be finally used in practical VLSI circuit designs as project deliverables. One of the two candidates will work primarily on the material preparation, fabrication and characterization while the other candidate will work primarily on the development of ML-driven device models and their VLSI circuit applications.

Duration of the project: 36 Months

Project position: Junior Research

Fellow**Number**: 02

Fellowship amount: 31,000 pm consolidated

Eligibility requirements: M.Tech., or M.E. (VLSI, Microelectronics, Nanotechnology, ECE, EEE andallied areas).

Interested candidates with the above mentioned minimum qualification can send their applications by email attaching their CV (in PDF format), furnishing detailed information about their educational qualifications, research experience and published research papers if any, by **Monday 1st August 2022**, to the Principal Investigator at **parikshit@hyderabad.bits-pilani.ac.in** with the subject line "**JRF Application**".

The candidate who will be selected for the material preparation, fabrication, and characterization profile must have a strong background in Device and Semiconductor Physics and Solid State Electronics. Prior experience in **Device Fabrication, Synthesis and Characterization of Nanomaterials** is desirable.

The candidate who will be selected for the VLSI device and circuit design profile must have the fundamental knowledge on electronic devices, basic circuit theory, and VLSI circuit designs. Candidates comfortable with device and circuit simulations with the basic hands-on knowledge on ML-based supervised learning algorithms using standard python tools are highly encouraged to apply.

Please note that only qualified and suitable candidates will be notified for Interview via email. Interview would be conducted online through Skype/Google Meet.

Selected candidates are recommended to pursue their full-time Ph.D. program of BITS, Pilani, subject tothe fulfillment of the official criteria.

Best Regards,

Dr. Parikshit Sahatiya

EEE Department, BITS Pilani Hyderabad Campus